# Sixth Semester B.E. Degree Examination, June/July 2014 Digital Communication 

Time: 3 hrs.
Max. Marks: 100

## Note: Answer FIVE full questions, selecting at least TWO questions from each part.

Importan Note : 1. On completing your answers. compulsorily draw diagonal cross lines on the remaining blank pages.

## PART - A

1 a. Explain natural sampling with relevant waveforms. Give all the necessary time-domain and frequency-domain equations.
(10 Marks)
b. What is aliasing error? Give two corrective measures to remove the effect of aliasing in practice.
(04 Marks)
c. Consider the analog signal $\mathrm{x}(\mathrm{t})=5 \cos (2000 \pi \mathrm{t})+10 \cos (6000 \pi \mathrm{t})$.
i) What is the Nyquist rate and Nyquist interval?
ii) Assume that if we sample the signal using sampling frequency $\mathrm{f}_{\mathrm{s}}=5000 \mathrm{~Hz}$, what is the resulting discrete time signal obtained after sampling?
iii) Draw the spectrum of the sampled signal.
(06 Marks)
2 a. Explain regencrative repeater in a PCM system with a block diagram.
(05 Marks)
b. The bandwidth of a signal is 3.4 kHz . If this signal is converted to PCM bit stream with 1024 levels, determine the number of bits per second (bps) generated by the PCM system. Assume that the signal is sampled at the rate of $20 \%$ above the Nyquist ratc. (06 Marks)
c. Dcrive an expression for the output SNR of a uniform quantizer in terms of step size of the quantizer. Hencc show that for mid-tread type uniform quantizer the SNR is $(S N R)_{\text {outpur }}=6 n-7.2 \mathrm{~dB}$, where ' $n$ ' is the number of bits per sample. Assume a loading factor of 4 .
(09 Marks)
3 a. Explain with block diagrams DPCM transmitter and receiver.
(09 Marks)
b. Explain briefly the basic optical fiber link used for the transmission of digital data. (06 Marks)
c. Show that for the bipolar format, the autocorrelation function $R_{a}(n)$, that is $E\left[A_{K} A_{K-n}\right]$ is zero for $n>1$, where $A_{K}$ is the $K^{\text {th }}$ random variable representing $K^{\text {th }}$ bit of the imput binary sequence. Assume statistically independent and equally likely message bits.
(05 Marks)
4 a. Explain raised cosine spectrum solution to reduce IS1.
(10 Marks)
b. The binary data 001101001 are applied to the input of the duobinary system.
i) Construct the duobinary coder output and the corresponding receiver output without a precoder.
ii) Suppose that due to error during transmission, the level at the receiver input produced by the second digit is reduced to zero. Construct the new receiver output.
( 10 Marks)

## PART - B

5 a. Explain the generation and demodulation of DPSK wave with block diagrams. ( 08 Marks)
b. Binary data are transmitted over a microwave link at the rate of $10^{6}$ bps and the PSD of the noise at the receiver input is $10^{-10} \mathrm{~W}$ atts per hertz. Find the average carrier power required to maintain an average probability of error $\mathrm{Pe} \leq 10^{-4}$ for coherent binary FSK. What is the required channel band width? (Take $\operatorname{crfc}(2.7)=2 \times 10^{-4}$ )
c. Explain briefly phase tree and phase Trellis in MSK.

# Sixth Semester B.E. Degree Examination, June/July 2014 Microprocessors 

Time: 3 hrs .
Max. Marks: 100

## Note: 1. Answer any FIVE full questions, selecting atleast TWO questions from each part. 2. Make suitable assumptions for any missing data.

## PART - A

1 a. Determine the appropriate register/memory locations that are used to compute the 5 digit hex address when the processor needs to address the contents of
i) Data segment memory.
ii) Program segment memory.
iii) Stack segment memory.
iv) Extra segment memory.
(08 Marks)
b. Explain the flag register of the processor in accordance with the respective bit positions.
(05 Marks)
c. Write an 8086 assembly code to copy the contents of flag register into accumulator register following any arithmetic or logical operation.
(07 Marks)
2 a. Explain the meaning of the following independent bits of 8086 assembly instruction templates: i) W -bit; ii) d-bit; iii) v-bit; iv) s-bit; v) z-bit.
(10 Marks)
b. Write an optimum number of assembly instructions for the following objectives. Also indicate the type of addressing mode used in each case.
i) Shift the contents of accumulator register 4 bits left.
ii) Rotate the contents of base register right by 2 bits.
iii) Divide the contents of accumulator register by 2 .
iv) Multiply the contents of base register by 4 .
v) If AL register contains a two digit BCD number, display the same on monitor using necessary DOS interrupts.
(10 Marks)
3 a. Consider that a symbolic memory address 'DISPTBL' contains a BCD to seven segment code starting from 4000 H to 400 AH . Design an assembly code to meet the following objectives:
i) Send a message to screen 'PRESS ANY KEY 0 to 9'.
ii) Read the key pressed from the key board.
iii) If invalid key is found, the program to loop back to step (i) with a suitable warning message.
iv) On correct key press, compute BCD to 7 segment code and store into memory location "DISPCODE'.
v) Use XLAT assembly instruction to achieve your objective.
vi) Design a suitable flow diagram to show your approach.
(10 Marks)
b. i) Differentiate between the usage of assembler directives MACRO and PROCEDURE.
ii) Develop a suitable MASM code to display minimum of 3 different line text message by using MACRO directive and PRINTF as macro name.
(10 Marks)

4 a. With reference to the internal architecture of 8086 processor. cxplain:
i) The different external sources external sources of hardware interrupts.
ii) How the processor checks to see an interrupt have been occurred.
iii) List of major aetions performed to process an interrupt.
(10 Marks)
h. Explain the following internal interrupts generated within the processor while executing the program:
i) TYPE-0 divide by zcro intcrrupt.
ii) TYPE-I single step interrupt.
(10 Marks)

## PART - B

5 a. With respect to programmable peripheral interface (PPI) 8255A:
i) Draw a ncat block schematic showing its functional description.
ii) Draw mode definition format the control word.
iii) Explain various possible modes of operation.
(10 Marks)
b. Design an 8255 hased cvent counting system. Port A is connceted to 8LEDs and Port B is comected to a toggling switch having 2 positions for binary and BCD. Draw the interfacing diagram and a program for binary or $B C D$ count as selected by switeh. Given that the control port address is 50 B 3 , assume safe current to glow each LED is 25 mA . A suitable delay between counts is considered.
(10 Marks)
6 a. What is meant by numeric data processor 8087 (NDP)? What are the bencfits of interfacing the same with the host processor?
(04 Marks)
b. Explain briefly the role played by the following pins of 8087 during interaction.
i) Bus high cnable (BHE/S7).
ii) Status pins $(\overline{\mathrm{s} 2}, \overline{\mathrm{st}}, \overline{\mathrm{s} 0})$.
iii) Rcqucst/Grant $(\overline{\mathrm{RQ}} / \overline{\mathrm{GT}})$.
(06 Marks)
c. Consider the given decimal number 178.625 convert it into
i) Short - real format (single precision representation).
ii) Long-real format (double precision representation).
(04 Marks)
d. Write a program to calculate the volume of a spherc having radius of the sphere is specified. The result is to be stored in the memory location VOLUME. Volume of a sphere is given by $(4 / 3) *(\mathrm{Pi}) *\left(\mathrm{r}^{* *} 3\right)$.
(06 Marks)
7 a. Draw a schematic diagram when 8086 proccssor is operating in maximum mode configuration.
(06 Marks)
b. Explain the function performed by pins exclusive for minimum mode configuration.
i) HOLD and HLDA ; ii) $M / \overline{\mathrm{IO}}$; iii) $\overline{\mathrm{RD}}$; iv) $\overline{\mathrm{WR}}$; v) $\mathrm{MN} / \overline{\mathrm{MX}}$.
(08 Marks)
c. What is meant by PCI bus system? List out the significant characteristics of the PCl bus system.
(06 Marks)
8 a. Explain the memory bank system architecture for the 80386DX microprocessor with a block schematic. Explain how interleaved memory system is used for speed improvement.
( 10 Marks)
h. Draw the block schematic of the control register of 80386 microprocessor and explain the following special control bits of operation i) PG ; ii) ET ; iii) TS ; iv) EM ; v) MP ; vi) PE .
(10 Marks)

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## Sixth Semester B.E. Degree Examination, June/July 2014 Microelectronics Circuits

Time: 3 hrs .
Max. Marks: 100

## Note: Answer any FIVE full questions, selecting atleast TWO questions from each part.

## PART - A

1 a. With a neat diagram, derive the expression for $i_{D}$ in saturation and triode region. What happened to $i_{D}$ if the channel length modulation is considered?
b. Draw the large signal equivalent circuit model of NMOS and explain.
c. Determine the voltages at all nodes and the currents through all the branches of following circuit. Let $V_{1}=1 V$ and $\mathrm{kn}^{\prime}(\mathrm{W} / \mathrm{L})=1 \mathrm{~mA} / \mathrm{V}^{2}$. Neglect the channel - length modulation effect.
(06 Marks)


Fig.Q.l(c)
2 a. Show the development of the T equivalent - circuit model for the MOSFET from hybrid $\pi$ model without channel length modulation.
(06 Marks)
b. Draw the circuit of common-source amplifier with a source resistance. Draw its small signal equivalent circuit with $\gamma_{0}$ neglected. Obtain the expression for $V_{g s}, i d, v_{o}, A_{v}, A_{v o}$ and the overall voltage gain $\mathrm{G}_{\mathrm{v}}$.
(10 Marks)
c. What is scaling? Differentiate constant field scaling and constant-voltage scaling. (04 Marks)

3 a. Briefly explain about short channel effect due to scaling.
(06 Marks)
b. Compare NMOSFET and BJT in terms of
i) Current voltage characteristic.
ii) High frequency model.
iii) Output resistance.
(06 Marks)
c. Following figure shoes the high frequency equivalent circuit of a common-source MOSFET amplifier. The amplifier is fed with a signal generator Vsig having a resistance Rig. Resistance $R$ in is due to the biasing network. Resistance $R_{I}^{\prime}$ is the parallel equivalent of the load resistance RL, the drain bias resistance $\mathrm{R}_{\mathrm{D}}$, and the FET output resistance fro. Capacitors cos and gd are the MOSFET internal capacitance:
i) Draw the equivalent circuit at midband frequencies.
ii) Draw the circuit for determining the resistance seen by Cos.
iii) Draw the circuit for determining the resistance seen by Cod. For Rig $=100 \mathrm{~K} \Omega$, Ron $=420 \mathrm{~K} \Omega, \mathrm{Cgs}=\mathrm{Cgd}=1 \mathrm{pF}, \mathrm{gm}=4 \mathrm{~mA} / \mathrm{V}$, and $\mathrm{R}_{\mathrm{L}}^{\prime}=3.33 \mathrm{~K} \Omega$
iv) Find the mid band voltage gain $\mathrm{A}_{\mathrm{M}}-\mathrm{V}_{0} / \mathrm{V}$ sig.
v) Find the upper $3-\mathrm{dB}$ frequency $\mathrm{f}_{\mathrm{H}}$.
(08 Marks)


Fig.Q.3(c)
4 a. In common-gate amplifier with active load, obtain 3 - dB frequency $\mathrm{f}_{\mathrm{f}}$ using open circuit time constants. Draw the circuit required for determining Rgs and Red.
(08 Marks)
b. Draw the $C_{D}-C_{s}, C_{D}-C_{E}$ and $C_{D}-C_{a}$ configurations.
(06 Marks)
c. Draw an $I_{C}$ source follower circuit. Obtain its small signal equivalent circuit and obtain its voltage gain $A_{v}=\frac{V_{0}}{V_{1}}$.
(06 Marks)

## PART-B

5 a. Obtain common-gate and common-mode rejection ratio (CMRR) of the MOS differential amplifier. Also find the effect of $\mathrm{R}_{\mathrm{D}}$ mismatch on CMRR.
(12 Marks)
b. Draw the two-stage CMOS op-amp configuration and briefly explain. Obtain overall dc open-loop gain.
(08 Marks)
6 a. Briefly explain about
i) Voltage amplifier
ii) Current amplifier
iii) Trans conductance amplifier
iv) Trans resistance amplifier.
(08 Marks)
b. Explain about series-shunt feedback amplifier with diagram and obtain the expression for input impedance and output impedance.
(08 Marks)
c. Briefly explain about stability and pole locations.
(04 Marks)

7 a. Draw and explain about weighted summer capable of implementing summing coefficients of
both signs.

(06 Marks)

b. Explain about DC imperfections.

(04 Marks)

c. Write short notes on:
i) Antilogarithmic amplifiers.
ii) Analog multipliers.
(10 Marks)
8 a. Draw the CMOS realization of A 01 gate and explain with truth table.
(08 Marks)
b. Draw and explain the exclusive OR function using PUN and PDN.
c. What all are the parameters used to characterize the operation and performance of a logic circuit family.
(04 Marks)
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## Sixth Semester B.E. Degree Examination, June / July 2014 Antennas and Propagation

Time: 3 hrs .
Max. Marks: 100

## Note: Answer FIVE full questions, selecting at least TWO questions from each part.

## PART - A

1 a. Define the following terms with respect to antenna:
i) Gain
ii) Isotropic radiator
iii) Beam area
iv) Radiation resistance.
(08 Marks)

2 a. Derive an expression for power radiated from an isotropic point source with "sine squared power pattern". Also find directivity "D" and draw power pattern.
(06 Marks)
b. Find the power radiated and directivity for the unidirectional point sources, having the following point sources power patterns:
i) $\mathrm{U}=\mathrm{U}_{\mathrm{m}} \cos ^{2} \theta \sin ^{3} \phi, \quad 0 \leq \theta \leq \pi, 0 \leq \phi \leq \pi$
ii) $\mathrm{U}=\mathrm{U}_{\mathrm{m}} \sin ^{2} \theta \sin ^{3} \phi, 0 \leq \theta \leq \pi, 0 \leq \phi \leq \pi$
(06 Marks)
c. Eight point sources are spaced $\frac{\lambda}{6}$ apart. They have a phase difference of $\frac{\pi}{3}$ between adjacent elements. Obtain the field pattern. Also find BWFN and HPBW.
(08 Marks)
3 a. Show that the radiation resistance of a half wave $\left(\frac{\lambda}{2}\right)$ dipole antenna is $73 \Omega$.
(06 Marks)
b. Write an explanatory note on folded dipole antenna, giving neat figures.
(06 Marks)
c. A magnetic field strength of $20 \mu \mathrm{~A} / \mathrm{m}$ is required to be produced at a point 2.5 km from the antenna in the broadside plane, in free space. How much power is transmitted by,
i) a hertzian dipole, with $l=\frac{\lambda}{15}$.
ii) a half wave dipole and
iii) a monopole antenna.
(08 Marks)
4 a. Discuss the features of a loop antenna. Derive an expression for the far field components of a loop antenna.
(10 Marks)
b. Explain Babinet's principle with illustrations. Discuss features of complementary antennas, with neat figures.
(10 Marks)

## PART - B

5 a. With a neat figure, explain the working of Yagi-Uda antenna. Write the design formulae for different components, used in Yagi-Uda antenna. Also mention the applications of Yagi-Uda antennas.
(08 Marks)
b. Determine :
i) The length $L$ aperture ' $\mathrm{a}_{\mathrm{H}}$ ' and half angles in E and H planes for a pyramidal Horn antenna, for which $\mathrm{a}_{\mathrm{E}}=10 \lambda$. The horn is fed with a rectangular wave guide in $\mathrm{TE}_{10}$ mode. Let $\delta=\frac{\lambda}{12}$ in the E-plane and $\delta=\frac{\lambda}{6}$ in the H-plane.
ii) Calculate directivity ' $D$ '.
(08 Marks)
c. Write a note on Corner Reflector antenna.
(04 Marks)
6 a. Write notes on:
i) Plasma antenna.
ii) Embedded antenna.
(08 Marks)
b. With a neat sketch, explain the principle of lens antenna.
(06 Marks)
c. A paraboloid reflector of 2 m diameter is used at 10 GHz . Calculate the beam width between first nulls (BWFN) HPBW and gain in dB.
(06 Marks)
7 a. Discuss various forms of radio-wave propagation.
(08 Marks)
b. Derive the expression for resultant electric field strength ( $E_{R}$ ) at a point, due to space wave propagation.
(06 Marks)
c. Derive the expression for 'Line of sight' distance (LOS) between transmitting and receiving antennas.
(06 Marks)
8 a. A high frequency radio link is to be established between two points on the earth 350 km apart. The reflection region of the atmosphere is at a height of 250 km and has a critical frequency of 8 MHz . Calculate the maximum usable frequency (MUF), for the given path in case of flat earth.
(06 Marks)
b. Define skip distance. Derive an expression for skip distance (D), for a flat earth. (06 Marks)
c. Define critical frequency. Find the critical frequency for a particular ionospheric layer with $\mathrm{Nm}=9 \times 10^{6} / \mathrm{cm}^{3}$. Also find maximum usable frequency (MUF), if the angle of incidence $\angle \mathrm{i}=60^{\circ}$
(08 Marks)
$\square$

# Sixth Semester B.E. Degree Examination, June/July 2014 Operating Systems 

Time: 3 hrs.
Max. Marks: 100

## Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART - A

1 a. Explain the goals of an operating system.
(06 Marks)
b. Explain the designer's view of operating system. (04 Marks)
c. Explain modes of performing 1/O operations. (05 Marks)
d. Explain the benefits/features of distributed operating system. (05 Marks)

2 a. Explain the functions of an operating system.
(05 Marks)
b. Explain the layered design of operating system.
(08 Marks)
c. Explain the concept of VMOS with example.
(07 Marks)
3 a. Explain the contents of process control block.
(06 Marks)
b. List the different types of process interaction and explain them in brief.
(06 Marks)
c. Explain with a neat diagram, the different states of process in UNIX operating system.
(08 Marks)
4 a. Describe static and dynamic memory allocation.
(04 Marks)
b. Compare the contiguous and non-contiguous memory allocation.
(04 Marks)
c. What is boundary tag? Explain merging of free areas using boundary tags?
(08 Marks)
d. Explain the lazy buddy allocator.
(04 Marks)

## PART - B

5 a. Explain the important concepts in the operation of demand paging.
(12 Marks)
b. Find the number of page faults for following page refercnce string, using the FIFO and LRU page replacement policies.
Reference string: $5,4,3,2,1,4,3,5,4,3,2,1,5 .($ Assume page frames $=3$ )
(08 Marks)
6 a. Describe the different operations performed on files.
(08 Marks)
b. Explain the organization of sequential access and direct access files.
(08 Marks)
c. Describe file system actions during a file operation.
(04 Marks)
7 a. Compute mean turn around timc and mean weighted turn around time for following set of processes, using FCFS and SRN scheduling.
( 10 Marks)

| Processes | $\mathrm{P}_{1}$ | $\mathrm{P}_{2}$ | $\mathrm{P}_{3}$ | $\mathrm{P}_{4}$ | $\mathrm{P}_{5}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Arrival time | 0 | 2 | 3 | 5 | 8 |
| Service time | 3 | 3 | 2 | 5 | 3 |

b. Explain the process schedule with a neat schematic diagram.
(05 Marks)
c. Summarize the approaches to real time scheduling.
(05 Marks)
8 a. Explain Buffering of interprocess messages.
(06 Marks)
b. Describe the delivery of interprocess messages.
(06 Marks)
c. Write a short note on mailbox.
$\square$

# Sixth Semester B.E. Degree Examination, June/July 2014 Satellite Communication 

Time: 3 hrs.
Max. Marks:100

## Note: Answer FIVE full questions, selecting at least TWO questions from each part.

## PART - A

1 a. Illustrate basic structure of a satellite communication. List the applications. (06 Marks)
b. Explain briefly the various services provided by a satellite. (06 Marks)
c. With suitable diagram, compare Low Earth Orbit (LEO), Medium Earth Orbit (MEO), Gcostationary orbit (GEO) satellite and its parameters.
(08 Marks)
2 a. Explain what are the orbital perturbation that take place because of non-spherical earth.
(06 Marks)
b. Explain in detail six orbital elements.
(06 Marks)
c. Explain with neat diagram the Earth eclipse of satellite and sun transit outage.
(08 Marks)
3 a. Explain what is effective path length. Show that the Rain Attenuation in dB is given by $A_{p}=a R_{p}^{b} L_{p} r_{p}$ with a ncat diagram.
(08 Marks)
b. Explain different transmission losses in a satellite link.
(06 Marks)
c. A satellite link operating at 14 GHz has receiver feeder losses of 1.5 dB and a free space loss of 207 dB . The atmospheric absorption loss is 0.5 dB and the antenna pointing loss is 0.5 dB . Depolarization loss may be neglected. Calculate the total link lass for clear sky conditions"?
(06 Marks)
4 a. List out the major sub-systems required on satellite.
(06 Marks)
b. Explain attitude and orbit control system.
(06 Marks)
c. With a neat diagram explain telemetry, tracking command and monitoring system. (08 Marks)

## PART - B

5 a. Explain with block diagram a llome Terminal for DBS TV/FM reception.
(I0 Marks)
b. Explain with block diagram a transmit-receive earth station.
(I0 Marks)
6 a. Describe briefly the modes of interference in a satellite communication system. Distinguish between satellite and terrestrial interference.
(10 Marks)
b. Explain spade communication system with a neat diagram. Also, the channeling scheme for spade system.
(10 Marks)
7 a. Explain: i) Orbit spacing, ii) Power rating, iii) Bit rate for digital television.
(10 Marks)
b. Explain in detail very small aperture terminal (VSAT) and its applications.
(10 Marks)
8 Write short notes an:
a. Orbit communication
b. Pre-assigned FDMA
c. Iridium

